Reg No.:_____ Name:_____

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

Seventh Semester B.Tech Degree Regular and Supplementary Examination December 2021 (2015 Scheme)

**Course Code: CS405**
**Course Name: Computer System Architecture**

Max. Marks: 100 Duration: 3 Hours

**PART A**

***Answer all questions, each carries 4 marks.*** Marks

| | | | |
|---|---|---|---|
| 1 | | Explain implicit and explicit parallelism in parallel programming | (4) |
| 2 | | Explain NUMA model for Multiprocessor Systems | (4) |
| 3 | | State Amdahl's law. Write an expression for overall speedup. | (4) |
| 4 | | Differentiate between crossbar network and multiport memory. | (4) |
| 5 | | Explain different message routing schemes. | (4) |
| 6 | | Explain the factors speedup, efficiency and throughput of a k-stage linear pipeline. | (4) |
| 7 | | Differentiate between Carry save adder (CSA) and Carry propagation adder(CPA). | (4) |
| 8 | | Write short notes on internal data forwarding. | (4) |
| 9 | | What are the four context switching polices for multithreaded architecture? | (4) |
| 10 | | Explain distributed caching. | (4) |

**PART B**

***Answer any two full questions, each carries 9 marks.***

| | | | |
|---|---|---|---|
| 11 | a) | Discuss the Bernstein's conditions to detect parallelism among a set of processes. | (4) |
| | b) | Determine the parallelism embedded in the following statements and draw the dependency graphs. Also analyse the statements against Bernstein's Conditions. | (5) |

P1: P = Q x R

P2: M = G + P

P3: S = T + P

P4: P = L + M

P5: F = G ÷ R

12 a) Explain memory hierarchy. (3)

b) Consider the design of a three level memory hierarchy with the following specifications for memory characteristics: (6)

| **Memory Level** | **Access time** | **Capacity** | **Cost/Kbyte** |
|---|---|---|---|
| Cache | t1 = 25 ns | S1 = 512 Kbytes | C1 = $1.25 |
| Main memory | t2 = 905 ns | S2 = 32 Mbytes | C2 = $0.24 |
| Disk array | t3 = 4 ms | S3 = 39 Gbytes | C3 = $0.0002 |

Hit ratio of cache memory is h1=0.98 and a hit ratio of main memory is h2=0.9.

(i) Calculate the effective access time.

(ii) Calculate the total memory cost.

13 a) Explain Flynn's classification of computer architecture with diagrams. (5)

b) Explain the inclusion, coherence and locality of reference properties of memory hierarchy. (4)

## PART C

***Answer any two full questions, each carries 9 marks.***

14 a) Design an 8 input omega network using 2X2 switches as building blocks. Show the switch settings for the permutation $\pi 1$ = (0,6,4,7,3)(1,5)(2). Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context. (6)

b) Explain the significance of multiport memory. (3)

15 Consider the three-stage pipelined processor specified by the following reservation table and answer the following: (S indicate the stages)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| S1 | X | | | | | X | | X |
| S2 | | X | | X | | | | |
| S3 | | | X | | X | | X | |

1. List the set of forbidden latencies and the collision vector. (2)

2. Draw the state transition diagram showing all possible initial sequences without causing a collision in the pipeline. (3)

3. List all the simple and greedy cycles from the state diagram. (2)

4. Determine the minimal average latency (MAL). (2)

16 a) Explain Write –invalidate Snoopy Bus Protocol using write-through cache. (4)

b) Consider a 16-node hypercube network. Based on the E-cube routing algorithm, show how to route a message from node (0100) to node (1101). All intermediate nodes must be identified on the routing path. (5)

## PART D

***Answer any two full questions, each carries 12 marks.***

17 a) Explain the mechanisms for instruction pipelining. (7)

b) Illustrate multiply pipeline design. (5)

18 a) Explain the latency hiding techniques used in distributed shared memory multicomputers. (8)

b) Distinguish between static dataflow computers and dynamic dataflow computers. (4)

19 a) Explain the Tomasulo's algorithm for the dynamic instruction scheduling. (5)

b) What are the problems of asynchrony and their solutions in massively parallel processors? (7)

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