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**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), MAY 2019**

Course Code: CS202

Course Name: COMPUTER ORGANISATION AND ARCHITECTURE (CS, IT)

Max. Marks: 100

Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks

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|---|--|---|
| 1 | Explain one, two and three address instruction with an example for each. | 3 |
| 2 | List the steps involved in invoking a subroutine through the use of a link register. | 3 |
| 3 | Draw a 3 x 2 array multiplier. | 3 |
| 4 | Non-restoring division is faster than restoring division. Justify the statement. | 3 |

PART B

Answer any two questions, each carries 9 marks

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|---|---|---|
| 5 | List various addressing modes explain any four with an example for each. | 9 |
| 6 | a) Draw the diagram of a multi-bus organization with 3 buses. Write the control sequence for the instruction Add R4, R5, R6 for the above mentioned multi-bus organization. | 5 |
| | b) Give the sequence of control steps required to perform the operation Add [R3], R1 in a single-bus organization. | 4 |
| 7 | a) Divide $(1000)_2$ by $(11)_2$ using restoring division method. | 4 |
| | b) Illustrate the basic operational concepts in transferring data between main memory and processor with neat diagram. | 5 |

PART C

Answer all question, each carries 3 marks

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|----|---|---|
| 8 | What are vectored interrupts? | 3 |
| 9 | Give the functions of initiator and target controllers in SCSI bus. | 3 |
| 10 | Compare synchronous and asynchronous DRAM. | 3 |
| 11 | Define temporal locality and spatial locality. | 3 |

PART D

Answer any two questions, each carries 9 marks

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|----|---|---|
| 12 | a) Differentiate centralized and distributed bus arbitration mechanism used in DMA. | 4 |
| | b) Give the structure of a typical static RAM cell and explain its read and write operations. | 5 |

- 13 Differentiate serial port and parallel port. Draw the diagram of a bidirectional 8-bit parallel interface and explain its working. 9
- 14 Elaborate the various cache mapping techniques with an example for each. 9

PART E

Answer any four questions, each carries 10 marks

- 15 a) Write the Register Transfer Logic format for a conditional control statement. Give an example and explain the same. 4
- b) Mention the advantages of using a scratch pad memory. Draw the diagram of a processor that employs a scratch pad memory and explain the same. 6
- 16 a) Design an adder/subtractor circuit with one selection variable s and two inputs A and B . When $s = 0$ the circuit performs $A + B$. When $s = 1$ the circuit performs $A - B$ by taking 2's complement of B . 5
- b) Design a 4-bit combinational logic shifter with 2 control signals H_1 and H_0 that performs the following operations (bit values given in parenthesis are the values of control variables H_1 and H_0 respectively):- No shift (00), Shift-right (01), Shift-left (10), Transfer 0's to S (11). 5
- 17 a) Draw and explain the block diagram for a 4-bit complete accumulator 6
- b) Discuss about condition code bits in a 4 bit status register 4
- 18 Design a hard-wired control unit based on the one flip-flop per state method to add/subtract 2 signed numbers represented in the sign-and-magnitude form. 10
- 19 Explain the organization of a microprogrammed computer with a block diagram 10
- 20 Draw a neat block diagram of a microprogram sequencer and explain its working. 10
