Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree (S,FE) Examination January 2022 (2015 Scheme)

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1 Convert the following numbers from the given base to the bases indicated (3)

a) $(153.87)_{10}$ to Hexadecimal

b) $(127)_8$ to Decimal

c) $(11101.1001)_2$ to Octal

2 Differentiate digital systems and analogue systems. (3)

3 Represent +51 and -51 in 1's complement and 2's complement form (3)

4 Convert the following expression into sum of product and product of sum (AB + C) (B + C'D) (3)

PART B

Answer any two full questions, each carries 9 marks.

5 a) Represent the number 85.125 using the double-precision floating point format IEEE-754 standard. (5)

b) Find Subtraction of 1B06 and 77C using 15's complement method (4)

6 Simplify the following expressions using K-Map, and implement it with two-level NAND gate circuits: (9)

AB′ + ABD + ABD′ + A′C′D′ + A′BC′

7 Use tabulation method to identify the simplified Boolean expression for the function, F(A,B,C,D) = ∑m (0,1,2,3,5,7,8,10,12,13,15) (9)

PART C

Answer all questions, each carries 3 marks.

8 Give the design and circuit for a half adder (3)

9 Implement the function F(A, B, C, D) = ∑ (0, 1, 3, 5, 7, 10, 12, 13) using a 4 X 1 multiplexer (3)

10 Differentiate combinational and sequential circuits. (3)

11		Draw the schematic diagram of a 3-bit parallel adder. What is the drawback of this circuit?	(3)

PART D

Answer any two full questions, each carries 9 marks.

12		Explain how clocked sequential circuits can be designed with state equations, using an example	(9)
13	a)	Design and implement full subtractor by using only NAND gates.	(5)
	b)	Design a 2-bit magnitude comparator.	(4)
14	a)	Explain clocked sequential circuits with an example.	(4)
	b)	Draw and explain the logic circuit of 4-bit full adder with look ahead carry.	(5)

PART E

Answer any four full questions, each carries 10 marks.

15		Design a Modulo 9 Synchronous counter using T FFs	(10)
16		With neat timing diagram and sequence table explain the working of 4bit Johnson Counter using JK Flip flops.	(10)
17		Using the circuit diagrams explain types of shift registers	(10)
18	a)	Give any 2 applications of ROM	(3)
	b)	Explain static RAM and Dynamic RAM	(4)
	c)	Write a note on error detection and correction.	(3)
19		Implement the following Boolean functions using a $3 \times 4 \times 2$ PLA $F_1 (A, B, C) = (3, 5, 6, 7)$ and $F_2 (A, B, C) = (0, 2, 4, 7)$.	(10)
20		Write an HDL code for a half adder	(10)

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